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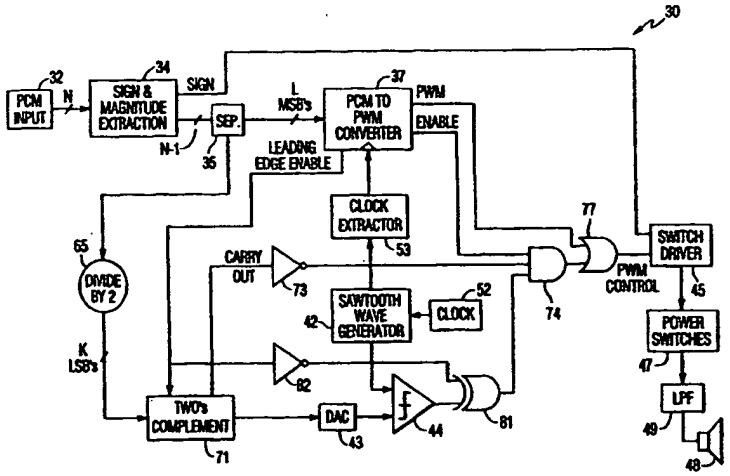

(57) Abstract

A class D amplifier includes a separating circuit for separating a pulse code modulation (PCM) signal into a K least significant bits (LSBs) signal and an L most significant bits (MSBs) signal; a PCM to pulse width modulation (PWM) converter for converting the L MSBs signal into a PWM signal; and an LSB processor for proportionally altering the PWM signal from the PCM to PWM converter based upon the K LSBs signal to define a PWM output control signal. The PCM input signal may be an N–1 bit PCM magnitude signal. The amplifier includes a sign and magnitude extraction circuit for extracting a sign bit signal and the N–1 bit magnitude signal from an N bit two's complement PCM input signal. The class D amplifier also includes a switch driver responsive to the extracted sign bit signal and the PWM output control signal, such as to control polarity and on time, respectively. The PCM to PWM converter may be one of a symmetric PCM to PWM converter; a trailing edge PCM to PWM converter; and a leading edge PCM to PWM converter.

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CLASS D AMPLIFIER WITH REDUCED CLOCK REQUIREMENT AND RELATED METHODS

The invention relates to the field of electronic circuits and devices, and, in particular, to a class D amplifier and related methods.

Amplifiers are widely used in many electronic devices to increase the input signal level to a desired output level. A class D amplifier includes an active device used as an on-off switch, and output power variations are achieved by pulse-width modulation. Class D amplifiers may be used in radio broadcast transmitters, and audio amplifiers. The very high switching efficiency of power metal-oxide field-effect transistors (MOSFETs), for example, permits their use in class D audio amplifiers to produce high fidelity signals with relatively compact and efficient circuits.

A typical digital input class D amplifier **10** is shown in FIG. 1. The amplifier **10** includes a digital format converter **11** which receives the input signal in a standard format. A sample rate converter **12** converts the output of the digital format converter for input to the pulse code modulation (PCM) to pulse width modulation (PWM) converter **13**. The output of the PCM to PWM converter **13** is coupled to the illustrated level shifter **14**, bridge **15**, and ultimately to a transducer **16**, such as a loudspeaker, for example. Reference number **17** illustrates various possible feedback paths for the amplifier **10**.

Unfortunately, a significant difficulty occurs in converting the high resolution PCM signal to a corresponding high resolution PWM signal. This is so because as the width of a pulse increases, it's direct current (dc) content increases with a one-to-one relationship. Each individual pulse has a sinc(x) frequency response. If the pulse repetition rate is high enough, then the low pass filter essentially only passes the dc component of each pulse and smooths the transition from one dc level to another as the dc values change as a function of time. Because this system is a sampled time system, the pulse widths are quantized in time as shown in the graphical plots of FIG. 2, where **P1-P5** are the illustrated pulses, and the upper plot **18** illustrates the pulse resolution clock edges. This PWM width quantization translates directly into a dc amplitude quantization. There is a practical limitation on the pulse resolution clock **18**, the clock that defines the pulse width quantization. This places an inherent limitation on the pulse width resolution which, in turn, limits the total harmonic distortion (THD) of the output signal.

For example, assuming a pulse repetition of 350 KHz, this repetition rate is high enough to support the operating assumption that the low pass filter at the amplifier's output is passing only the near dc signal component, while not being so high as to force a prohibitively high pulse resolution clock for lower resolutions. Higher resolutions are quite

different. For example, if it is desired to preserve 16 bits of accuracy through the PCM to PWM conversion, then the pulse repetition clock rate required is 350 KHz times 2^6 or 23 GHz. Such a high required clock rate is impractical.

One prior art approach to overcome this difficulty is to add a noise shaper or filter 21 to the processing chain upstream of the PCM to PWM converter 13 in the circuit 20 as shown in FIG. 3. The noise shaper 21 reduces the required resolution of the PCM signal, and, thus reduces the required time resolution of the subsequent PWM signal. The noise shaper 21 does this by weighting the quantization noise toward the ultimately rejected higher frequencies, and uses the high frequency noise to dither the signal of interest through the low resolution PCM to PWM converter 13. The input signal has an N bit resolution and the output signal has an M bit resolution, where N is greater than M. The ability of the noise shaper 21 to shape the noise is based upon the fact that adjacent input samples are highly correlated. This correlation is assured by the preceding interpolation in the sample rate conversion block 12.

The output signal-to-noise ratio (SNR) can be increased by increasing the degree of oversampling of the input signal, or increasing the order of the noise shaping filter 21. Unfortunately, increasing the degree of oversampling drastically increases overall system complexity, while increasing the noise shaping filter's order beyond three offers diminishing improvement in performance at reasonable oversampling rates. One source of increased system complexity occurs because interpolation filter complexity must be increased.

Another difficulty arises because increasing the oversampling increases the PWM repetition rate. Thus, to keep the same pulse resolution clock rate, one less bit is allowed in the quantizer for every factor of two that the sampling rate is increased. This may mean that for a third order noise shaping filter, a net noise floor gain of approximately 1.6 bits is realized for every factor of two that the sampling rate is increased, and assuming ideal interpolation.

Yet another difficulty with a conventional noise shaping filter 21 is based upon the dithering noise that must be carried through the PCM to PWM converter 13 to decrease the required PWM timer resolution. This dithering may be later removed by the low pass filter 22. However, there may be perceptible effects in sound quality that result from the dithering. The present invention includes a class D amplifier comprising input means for receiving an N bit two's complement pulse code modulation (PCM) input signal, sign and magnitude extraction means for extracting a sign bit signal and an N-1 bit magnitude signal from the N bit two's complement PCM input signal, separating means for separating the N-1

bit magnitude signal into a K least significant bits (LSBs) signal and an L most significant bits (MSBs) signal, a PCM to pulse width modulation (PWM) converter for converting the L MSBs signal into a PWM signal, LSB processing means for proportionally altering the PWM signal from said PCM to PWM converter based upon the K LSBs signal to define a PWM output control signal, and a switch driver responsive to the extracted sign bit signal and the PWM output control signal.

An object of the present invention is to provide a class D amplifier and associated methods having reduced or eliminated requirements for a noise shaping circuit, comprising: separating means for separating a pulse code modulation (PCM) signal into a K least significant bits (LSBs) signal and an L most significant bits (MSBs) signal; a PCM to pulse width modulation (PWM) converter for converting the L MSBs signal into a PWM signal; and LSB processing means for proportionally altering the PWM signal from the PCM to PWM converter based upon the K LSBs signal to define a PWM output control signal. More particularly, the PCM input signal may be an N-1 bit PCM magnitude signal. Accordingly the amplifier preferably further includes sign and magnitude extraction means for extracting a sign bit signal and the N-1 bit magnitude signal from an N bit two's complement PCM input signal. The class D amplifier may also include a switch driver responsive to the extracted sign bit signal and the PWM output control signal, such as to control polarity and on time, respectively.

The PCM to PWM converter may be one of a symmetric PCM to PWM converter; a trailing edge PCM to PWM converter; and a leading edge PCM to PWM converter. Thus, the LSB processing means preferably comprises means for cooperating with the respective type of PCM to PWM converter.

The LSB processing means may comprise a sawtooth wave generator for generating a sawtooth wave signal; a digital-to-analog converter (DAC) for converting a signal related to the K LSBs magnitude signal into an analog signal; and a comparator for generating a threshold signal based upon a comparison of the sawtooth wave signal and the analog signal. The LSB processing means may further comprise logic means for generating the PWM control signal based upon the threshold signal and the PWM signal. In addition, the amplifier may further include a reference clock connected to the sawtooth wave generator, and clock extracting means operatively connected between the sawtooth generator and the PCM to PWM converter for synchronizing conversion. The invention also includes a A "Y" method for operating class D amplifier comprising the steps of separating a pulse code modulation (PCM) signal into a K least significant bits (LSBs)

signal and an L most significant bits (MSBs) signal; converting the L MSBs signal into a PWM signal; and proportionally altering the PWM signal based upon the K LSBs signal to define a PWM output control signal, in which the PCM input signal is an N-1 bit PCM magnitude signal; and further comprising the steps of extracting a sign bit signal and the N-1 bit magnitude signal from an N bit two's complement PCM input signal, including the step of operating a switch driver responsive to the extracted sign bit signal and the PWM output control signal.

A method aspect of the invention is for operating a class D amplifier. The method comprises the steps of: separating a pulse code modulation (PCM) signal into a K least significant bits (LSBs) signal and an L most significant bits (MSBs) signal; converting the L MSBs signal into a PWM signal; and proportionally altering the PWM signal based upon the K LSBs signal to define a PWM output control signal. The PCM input signal may be an N-1 bit PCM magnitude signal. Accordingly, the method may further comprise the steps of extracting a sign bit signal and the N-1 bit magnitude signal from an N bit two's complement PCM input signal, and operating a switch driver responsive to the extracted sign bit signal and the PWM output control signal. The invention will now be described, by way of example, with reference to the accompanying drawings in which:

FIG. 1 is a schematic block diagram of a class D amplifier according to the prior art.

FIG. 2 is a plot of the PWM pulses and the pulse resolution clock signal for the class D amplifier as in the prior art of FIG. 1.

FIG. 3 is a schematic block diagram of a class D amplifier according to the prior art and including a noise shaper.

FIG. 4 is a schematic block diagram of one embodiment of a class D amplifier in accordance with the present invention.

FIG. 5 is a timing diagram of signals produced by the embodiment of the invention shown in FIG. 4.

FIG. 6 is a schematic block diagram of another embodiment of a class D amplifier in accordance with the present invention.

FIG. 7 is a timing diagram of signals produced by the embodiment of the invention shown in FIG. 6.

FIG. 8 is a timing diagram of signals produced by a variation of the embodiment of the invention shown in FIG. 6.

Like numbers refer to like elements throughout.

Referring to FIGS. 4 and 5, a first embodiment of the class D amplifier 30 includes input means 32 for producing an N bit, two's complement, PCM signal in the illustrated embodiment. The invention contemplates other than two's complement inputs as well. The first embodiment of the class D amplifier 30 is also configured for symmetric modulation for the purposes of illustration.

The N bit PCM input signal is first illustratively processed by the sign and magnitude extractor 34 which produces a sign bit signal, and an N-1 bit magnitude signal as will also be readily appreciated by those skilled in the art. Downstream from the sign and magnitude extractor 34, separating means 35 is provided for separating an N-1 bit PCM signal into a K least significant bits (LSBs) signal and an L most significant bits (MSBs) signal. The sign bit signal is fed to the switch driver 45 where the final PWM signal interval will be appropriately formatted. The sizes of L and K are determined based upon a tradeoff between the complexity of the circuits used to operate on the two words.

The class D amplifier 30 also includes the schematically illustrated PCM to PWM converter 37 for converting the L MSBs signal. The PCM to PWM converter 37 may include one or more counters, dependent on the type of PWM used, preset to an L dependent value clocked by the pulse resolution clock. The counters turn the modulated pulse on or off at predetermined times dependent on L and the pulse repetition rate. In the embodiment, the counters of the PCM to PWM converter 37 are driven by a clock signal which is synchronous with a sawtooth wave generator 42 used to process the K LSBs word or signal. The PCM to PWM converter 37 produces a PWM signal.

The amplifier 30 also includes LSB processing means for proportionally altering the PWM signal from the PCM to PWM converter 37 based upon the K LSBs signal to define a PWM output control signal which is input to the switch driver 45. The switch driver 45 is responsive to the extracted sign bit signal and the PWM output control signal to control polarity and on time, respectively, for the switch driver. The switch driver 45 may also be coupled to the schematically illustrated power switches 47 which, in turn, may be coupled to a transducer, such as the illustrated audio speaker 48.

The PCM to PWM converter may be one of a symmetric PCM to PWM converter; a trailing edge PCM to PWM converter; and a leading edge PCM to PWM converter. Thus, the LSB processing means preferably comprises means for cooperating with the respective type of PCM to PWM converter. For the class D amplifier 30, the PCM to PWM converter 37 is a symmetric converter.

The LSB processing means comprises a sawtooth wave generator 42 for

generating a sawtooth wave signal; a digital-to-analog converter (DAC) **43** for converting a signal related to the K LSBs magnitude signal into an analog signal; and a comparator **44** for generating a threshold signal based upon a comparison of the sawtooth wave signal and the analog signal. The LSB processing means may further comprise logic means for generating the PWM control signal based upon the threshold signal and the PWM signal. In addition, the class D amplifier **30** further includes the illustrated reference clock **52** connected to the sawtooth wave generator **42**; and clock extracting means **53** operatively connected between the sawtooth generator and the PCM to PWM converter **37** for synchronizing conversion.

For the illustrated embodiment of symmetric PWM, the result of the LSB processing is enabled one clock edge before the onset of a pulse generated by the MSB processing and is disabled one clock edge after a pulse is turned off by the MSB processing. This is illustrated by the blocks **61, 62** in FIG. 5. The figure also shows the sawtooth wave **67** produced by the generator **42**. If all of the MSB magnitude bits are zero, for example, the LSB processing circuit is enabled for only two clock periods.

The K LSBs signal of the N-1 PCM signal is used to drive an analog threshold circuit which is used to turn the PWM pulse on and off in the pulse resolution clock time just prior or just after the onset or end of the PCM to PWM converter **37** generated pulse. The actual on and off times are directly proportional to the LSB PCM value as will be readily appreciated by those skilled in the art. Accordingly, the combination of the sign bit, MSB and LSB signal processing chains thus give an accurate N bit PCM to PWM conversion.

The class D amplifier **30** is understood with reference to the following example. Assume a pulse repetition rate of 352.8 KHz with a 177 ns dead time (1/16 of the pulse repetition period), so that the maximum pulse duration is 15/16 X 1/352.8 KHz = 2.657 μs. Further assume that L is selected to be seven bits, then the pulse resolution clock frequency is 48.16896 MHz and the clock period is 20.76 ns. Assume that the desired pulse width is 238.74 ns or 11.5 clock periods, and assume that the pulse is negative. The input binary value is 1111010010000000. The sign bit is stripped off and sent to the switch driver **45** as previously described. Thus, when the pulse output is off, the class D amplifier's output will be 0 volts, and when the pulse output is turned on, the output will be -V volts. The sign extraction circuit **34** takes the magnitude of the input and sends 0001011 to the PCM to PWM converter **37** and 10000000 to the divider **65**.

The divider **65** is used for symmetric PWM because the pulse width

contributed by the LSBs needs to be equally divided between the leading and trailing pulse edges. This division can be thought of as schematic only, and may also be implemented by threshold scaling.

The PCM to PWM converter 37 turns on a pulse for 11 clock counts as indicated by the vertical marks 66 in FIG. 5. It is the task of the LSB processing to generate an output three quarters of the way into the first enabled clock period and to turn off its output one quarter of the way into the last enabled clock as also shown in FIG. 5.

The sawtooth wave 67 used in the example rises on the leading edge. Because the analog comparator 44 compares a converted version of the K bit PCM signal to a sawtooth wave, and because the smaller the PCM value the earlier the comparator should trigger, the K bit digital word is first two's complemented by the circuit 71. The two's complement output is used during the leading edge enable period only. Because of the special case when all K bits are equal to zero, the two's complement carry out signal is used to disable the output of the comparator 44 via the illustrated inverter 73 and AND gate 74. In other words, the if a K bit value of zero is received, then the LSB processing circuit should not activate. However, the K bit two's complement value of zero is zero and the circuit would trigger at the beginning of the clock signal cycle, thus the need for the disable signal.

During the trailing edge enable period, the output of the comparator 44 is inverted to compensate for the leading edge rise on the sawtooth wave 67. FIG. 5, describes where the sawtooth wave 67 is seen to be below the threshold of the comparator during the period when the LSBs processing circuit needs to enable the trailing part of the output pulse. This also accounts for the case when the LSBs are equal to zero. Of course, the output of the two's complement circuit 71, whether enabled (complementing) or disabled (pass through) is passed to a low resolution DAC 43 where the PCM signal is converted to an analog format. The output of the DAC 43 may require some degree of filtering to smooth the output signal. Such as output filter would not be used for signal reconstruction, but for signal accuracy so that it would not have the same constraints as the typical DAC anti-imaging filter.

The analog signal is fed to the comparator 44 where it is compared to a linearly increasing waveform 67 in this illustrated embodiment. When one input is greater than or equal to the other signal, then an output signal is generated. The leading edge enable signal from the PCM to PWM converter 37 is also coupled to the exclusive OR gate 81 via the illustrated inverter 82. The exclusive OR gate 81 also receives as an input, the

output of the comparator 44.

The combination of the DAC 43, comparator 44, and sawtooth waveform generator 42 described herein could be replaced with any device/circuit that generates an output signal delayed from a time reference, where the delay is linearly proportional to the input digital value.

Once the output of the comparator 44 is gated by the enabling signals described above, it is ORed with the output of the PCM to PWM converter 37 in the illustrated OR gate 77 to form the desired final pulse width. It is assumed that the two input signals to the OR gate 77 are synchronized by the clock extraction circuit 53. The switch driver 45 translates the PWM signal into a format compatible with the actual power switches 47. The power switches 47 may be coupled to a transducer, such as the illustrated loudspeaker 48 via the illustrated low pass filter 49.

Turning now to FIGS. 6 and 7, a second embodiment of the class D amplifier 30' is now described. This embodiment includes similar components as those described above and as indicated with prime notation. This embodiment is a representation also directed to a two's complement input. This embodiment of the class D amplifier 30' also assumes trailing edge modulation and trinary pulses.

An N bit two's complement PCM signal is fed to the sign and magnitude extraction circuit 34'. The sign is fed to the switch driver 45'. The magnitude output is an N-1 bit magnitude value which is then divided or separated by the separator circuit 35' into an L bit MSB word and a K bit LSB word. The selection of L and K may be made based upon a consideration of the tradeoff between circuit complexity in the various portions of the class D amplifier 30'.

The truncated PCM magnitude value L is fed to an L bit PCM to PWM converter 37'. The counters of the converter 37' are driven by a clock which is synchronous with a wave generator used to process the LSB word as illustrated in the timing diagram of FIG. 7. For the illustrated embodiment, trailing edge PWM is used so that the result of the LSB processing is disabled one clock edge after a pulse is turned off the by the MSB processing. This is understood with reference to the block 80 in FIG. 7. If all of the MSB magnitude bits are zero, the LSB processing circuit is enabled for only one clock period.

The K LSBs signal of the N-1 bit PCM magnitude is used to drive the analog threshold circuit which, in turn, is used to turn the PWM pulse off in the pulse resolution clock period just after the end of the pulse generated by the PCM to PWM converter 37'. The actual off time is directly proportional to the LSB PCM value. In summary, the

combination of the sign bit, MSB and LSB signal processing chains thus give an accurate N bit PCM to PWM conversion.

Turning to a practical example, assuming a pulse repetition rate of 352.8 KHz with a 177 ns dead time (1/16 of the pulse repetition period), the maximum pulse duration is 15/16 X 1/352.8 KHz = 2.657 μs. If it is further assumed that L is selected as seven, then the pulse resolution clock frequency is 48.16896 MHz and the clock period is 20.76 ns.

Further assume that the desired pulse width is 238.74 ns or 11.5 clock periods and assume that the pulse is positive. The input binary value is 0000101110000000. The sign bit is stripped off and sent to the switch driver **45'**. Thus, when the pulse output is off, the class D amplifier's output will be 0 volts, and when the pulse output is turned on, the amplifier's output will be V volts. The sign and magnitude extractor **34'** and separator **35'** sends 0001011 to the PWM to PCM converter **37'** and 10000000 to the DAC **43'** in the LSB processing circuit portion. The output of the DAC **43'** may benefit from some degree of filtering to smooth the output signal.

The analog signal is fed to the comparator **44'** where it is compared to a linearly increasing waveform as shown in FIG. 7. When the input from the DAC **43'** is greater than or equal to the sawtooth waveform **67'**, then an output signal is generated. The combination of the DAC **43'**, comparator **44'**, and sawtooth wave generator **42'** could be replaced with an equivalent circuit that generates an output signal delayed from a time reference, and where the delay is linearly proportional to the input digital value.

In the case of the illustrated embodiment and example, the PCM to PWM converter **37'** turns on a pulse for 11 clock counts, and enables the LSB processing circuit output one clock edge after those 11 clock periods. The LSB processing generates an output half of the way into the first enabled clock time, and turns off its output as shown in FIG. 7.

Once the output of the comparator **44'** is gated by the enabling signals described above via the AND gate **81**, it is ORed in the OR gate **82** with the output o the PCM to PWM converter **37'** to form the desired final pulse width. It is assumed that the two input signals to the OR gate **82** are synchronized by the clock extraction circuitry. The resulting signal is fed to the switch driver **45'**. Those elements noted with a prime and not specifically described with reference to FIG. 6, have been fully described above with reference to FIG. 4, and, hence, these elements need no further description.

Turning additionally to the timing diagram of FIG. 8, another embodiment of the class D amplifier **30"** is now explained. This embodiment is directed to leading edge

modulation. The circuit may be readily implemented using a circuit similar to that shown in FIG. 6; however, for leading edge modulation, the sawtooth wave generator generates a sawtooth wave 85 that decreases from the leading edge as shown in FIG. 8. In this embodiment, the LSB processing circuit is enabled one clock cycle before the PCM to PWM converter 37' triggers the onset of a pulse. The LSB enable area is shown by the box 86 in FIG. 8. As can be readily determined from FIG. 8, the LSB circuit fires when the voltage output of the DAC 43' is greater than the corresponding portion of the sawtooth wave 85.

A method aspect of the invention is for operating a class D amplifier. The method comprises the steps of: separating a pulse code modulation (PCM) signal into a K least significant bits (LSBs) signal and an L most significant bits (MSBs) signal; converting the L MSBs signal into a PWM signal; and proportionally altering the PWM signal based upon the K LSBs signal to define a PWM output control signal. The PCM input signal may be an N-1 bit PCM magnitude signal. Accordingly, the method may further comprise the steps of extracting a sign bit signal and the N-1 bit magnitude signal from an N bit two's complement PCM input signal, and operating a switch driver responsive to the extracted sign bit signal and the PWM output control signal.

A class D amplifier includes a separating circuit for separating a pulse code modulation (PCM) signal into a K least significant bits (LSBs) signal and an L most significant bits (MSBs) signal; a PCM to pulse width modulation (PWM) converter for converting the L MSBs signal into a PWM signal; and an LSB processor for proportionally altering the PWM signal from the PCM to PWM converter based upon the K LSBs signal to define a PWM output control signal. The PCM input signal may be an N-1 bit PCM magnitude signal. The amplifier includes a sign and magnitude extraction circuit for extracting a sign bit signal and the N-1 bit magnitude signal from an N bit two's complement PCM input signal. The class D amplifier also includes a switch driver responsive to the extracted sign bit signal and the PWM output control signal, such as to control polarity and on time, respectively. The PCM to PWM converter may be one of a symmetric PCM to PWM converter; a trailing edge PCM to PWM converter; and a leading edge PCM to PWM converter.

CLAIMS:

1. A class D amplifier comprising input means for receiving an N bit two's complement pulse code modulation (PCM) input signal, sign and magnitude extraction means for extracting a sign bit signal and an N-1 bit magnitude signal from the N bit two's complement PCM input signal, separating means for separating the N-1 bit magnitude signal into a K least significant bits (LSBs) signal and an L most significant bits (MSBs) signal, a PCM to pulse width modulation (PWM) converter for converting the L MSBs signal into a PWM signal, LSB processing means for proportionally altering the PWM signal from said PCM to PWM converter based upon the K LSBs signal to define a PWM output control signal, and a switch driver responsive to the extracted sign bit signal and the PWM output control signal.

2. A class D amplifier as described in Claim 1 wherein said PCM to PWM converter is a symmetric PCM to PWM converter; and said LSB processing means comprises means for cooperating with said symmetric PCM to PWM converter.

3. A class D amplifier as described in Claim 1 wherein said PCM to PWM converter is a trailing edge PCM to PWM converter; and said LSB processing means comprises means for cooperating with said trailing edge PCM to PWM converter.

4. A class D amplifier as described in Claim 1 wherein said PCM to PWM converter is a leading edge PCM to PWM converter; and said LSB processing means comprises means for cooperating with said leading edge PCM to PWM converter.

5. A class D amplifier as described in Claim 1 wherein said LSB processing means comprises a sawtooth wave generator for generating a sawtooth wave signal, a digital-to-analog converter (DAC) for converting a signal related to the K LSBs signal into an analog signal, a comparator for generating a threshold signal based upon a comparison of the sawtooth wave signal and the analog signal, and said LSB processing means further comprises logic means for generating the PWM output control signal based upon the threshold signal and the PWM signal, in which said logic means comprises an "OR" gate.

6. A class D amplifier as described in Claim 5 a reference clock connected to said sawtooth wave generator, clock extracting means operatively connected between said sawtooth generator and said PCM to PWM converter for synchronizing conversion thereof, said PCM to PWM converter includes first enable means for generating a first enable signal for use by said logic means, in which said LSB processing means includes divide by two means for dividing the K LSBs magnitude signal by two, two's complement means connected between said divide by two means and said DAC, and said two's

complement means has a carry output, and said logic means comprises a first inverter connected to the carry output, and preferably said PCM to PWM converter comprises enable means for generating a second enable signal coupled to said two's complement means and to said logic means, which said logic means comprises a second inverter receiving the second enable signal,

7. A class D amplifier as described in Claim 1 wherein said switch driver has a controllable polarity responsive to the extracted sign bit signal, in which said switch driver has an on time responsive to the PWM output control signal with at least one power switch connected to said switch driver.

8. A class D amplifier comprising separating means for separating a pulse code modulation (PCM) signal into a K least significant bits (LSBs) signal and an L most significant bits (MSBs) signal, a PCM to pulse width modulation (PWM) converter for converting the L MSBs signal into a PWM signal, LSB processing means for proportionally altering the PWM signal from said PCM to PWM converter based upon the K LSBs signal to define a PWM output control signal, the PCM input signal is an N-1 bit PCM magnitude signal; and comprising sign and magnitude extraction means for extracting a sign bit signal and the N-1 bit magnitude signal from an N bit two's complement PCM input signal, in which a switch driver responsive to the extracted sign bit signal and the PWM output control signal, and said switch driver has a controllable polarity responsive to the extracted sign bit signal; and wherein said switch driver has an on time responsive to the PWM output control signal.

9. A class D amplifier comprising sign and magnitude extraction means for extracting a sign bit signal and an N-1 bit magnitude signal from an N bit two's complement PCM input signal, separating means for separating the N-1 bit magnitude signal into a K least significant bits (LSBs) signal and an L most significant bits (MSBs) signal, a PCM to pulse width modulation (PWM) converter for converting the L MSBs signal into a PWM signal, LSB processing means for proportionally altering the PWM signal from said PCM to PWM converter based upon the K LSBs signal to define a PWM output control signal, said LSB processing means comprising a sawtooth wave generator for generating a sawtooth wave signal, a digital-to-analog converter (DAC) for converting a signal related to the K LSBs signal into an analog signal, a comparator for generating a threshold signal based upon a comparison of the sawtooth wave signal and the analog signal, logic means for generating the PWM output control signal based upon the threshold signal and the PWM signal, and clock extracting means operatively connected

between said sawtooth generator and said PCM to PWM converter for synchronizing conversion thereof, and a switch driver responsive to the extracted sign bit signal and the PWM output control signal, in which said PCM to PWM converter is a symmetric PCM to PWM converter; and wherein said LSB processing means comprises means for cooperating with said symmetric PCM to PWM converter, and preferably said PCM to PWM converter is a trailing edge PCM to PWM converter; and wherein said LSB processing means comprises means for cooperating with said trailing edge PCM to PWM converter.

10. A "Y" method for operating class D amplifier comprising the steps of: separating a pulse code modulation (PCM) signal into a K least significant bits (LSBs) signal and an L most significant bits (MSBs) signal; converting the L MSBs signal into a PWM signal; and proportionally altering the PWM signal based upon the K LSBs signal to define a PWM output control signal, in which the PCM input signal is an N-1 bit PCM magnitude signal; and further comprising the steps of extracting a sign bit signal and the N-1 bit magnitude signal from an N bit two's complement PCM input signal, including the step of operating a switch driver responsive to the extracted sign bit signal and the PWM output control signal.

11. A method as described in Claim 10 wherein the converter step comprises symmetrically converting the L MSBs signal into the PWM signal, in which the converter step comprises converting using trailing edge conversion, and preferably the converter step comprises converting using leading edge conversion.

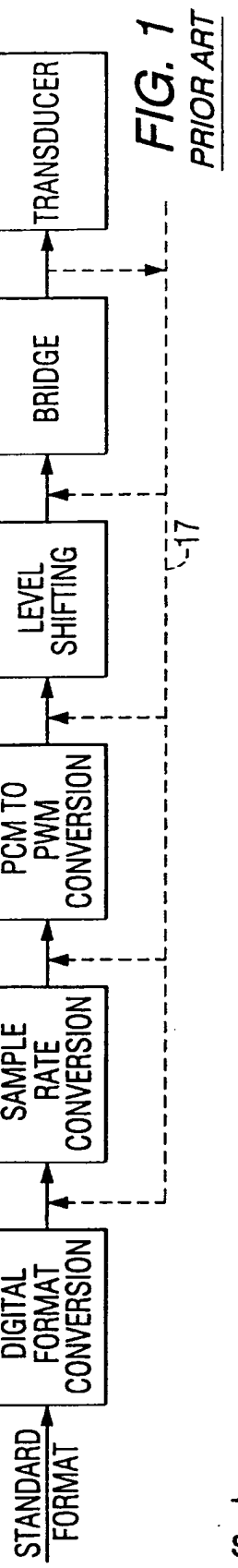

FIG. 1
PRIOR ART

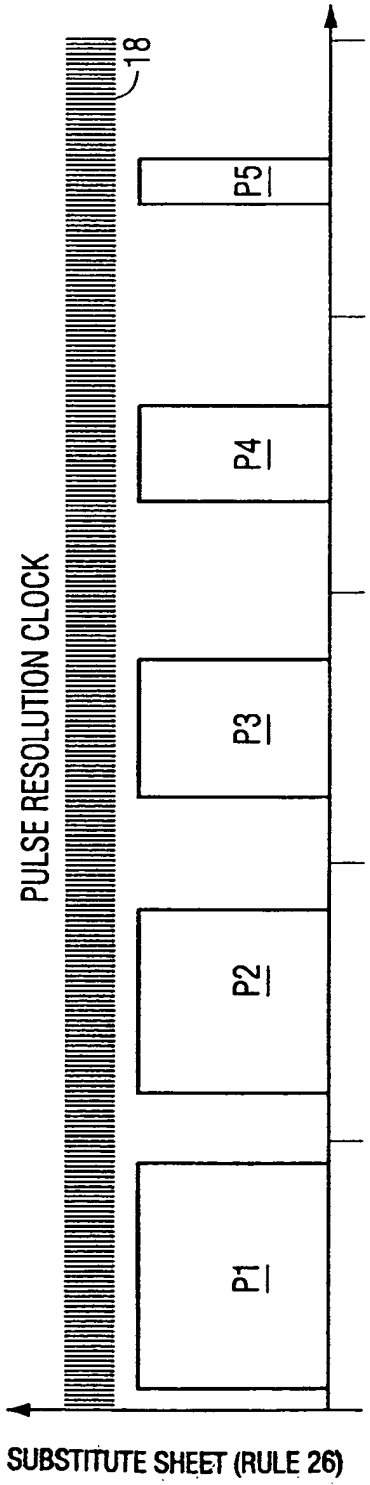

FIG. 2
PRIOR ART

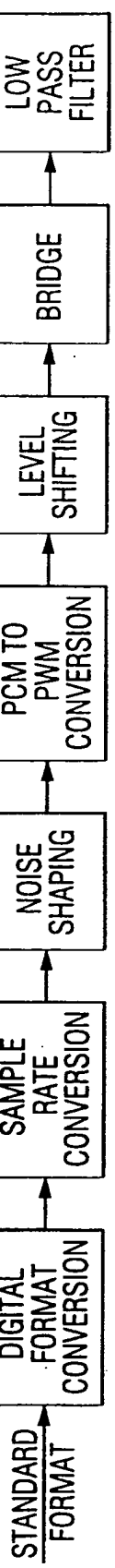

FIG. 3
PRIOR ART

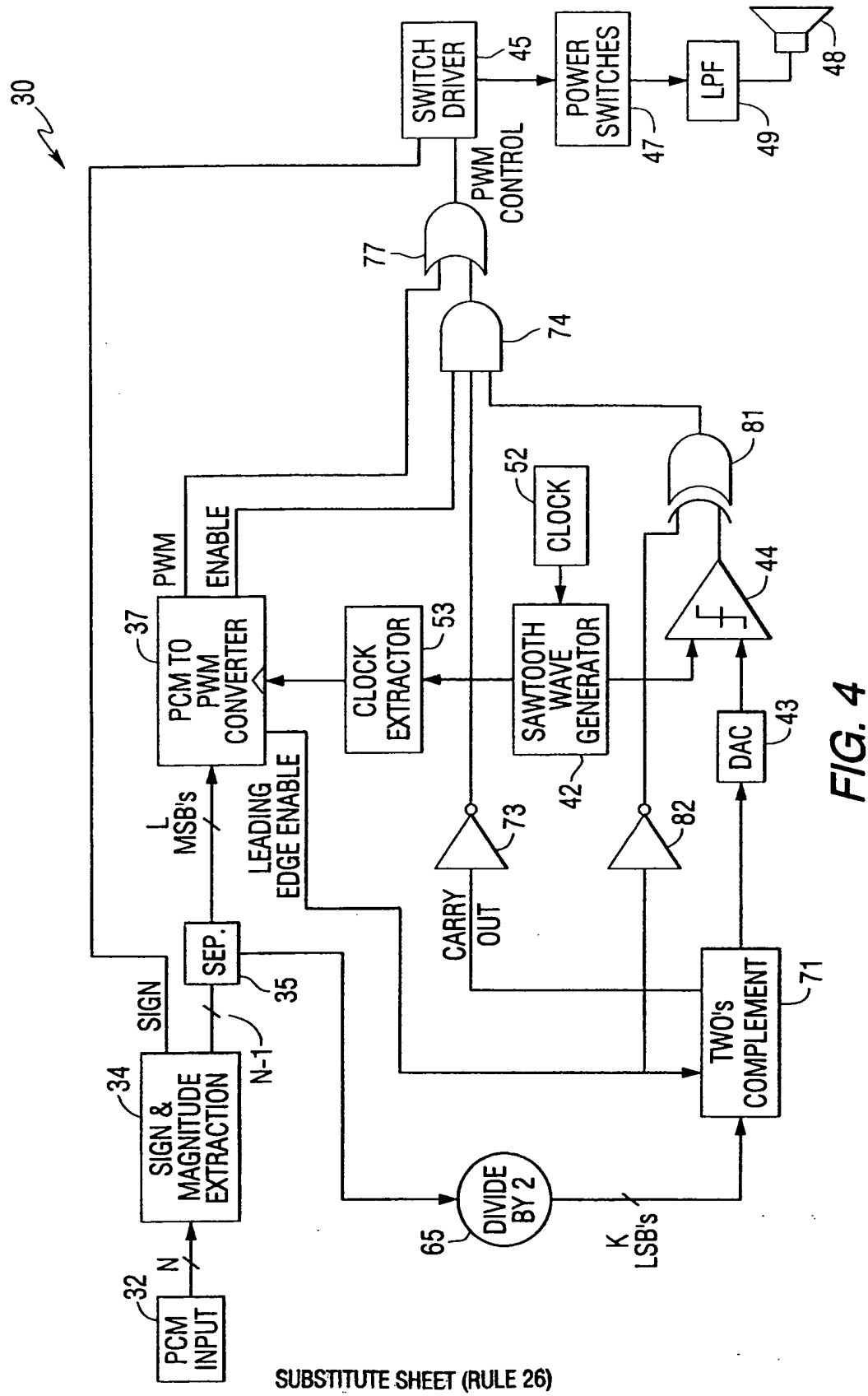
30
SWITCH DRIVER
45
POWER SWITCHES
47
LPF
49
48
PWM CONTROL
77
74
81
52
CLOCK
44
PWM
ENABLE
37
PCM TO PWM CONVERTER
CLOCK EXTRACTOR
53
SAWTOOTH WAVE GENERATOR
42
DAC
43
L MSB's
LEADING EDGE ENABLE
73
82
CARRY OUT
SEP.
35
SIGN
N-1
34
SIGN & MAGNITUDE EXTRACTION
TWO's COMPLEMENT
71
65
DIVIDE BY 2
K LSB's
32
N
PCM INPUT

FIG. 4

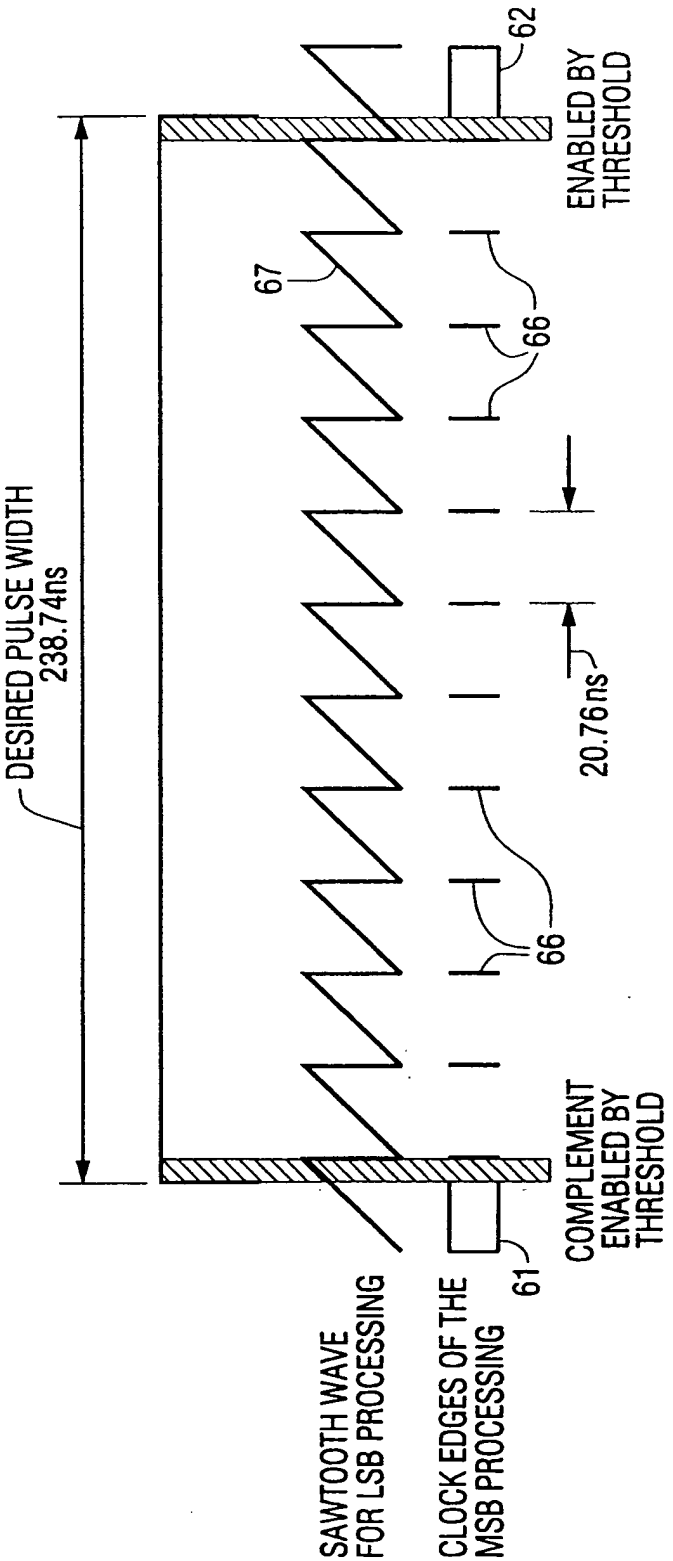
62
ENABLED BY THRESHOLD
67
66
66
DESIRED PULSE WIDTH 238.74ns
20.76ns
66
COMPLEMENT ENABLED BY THRESHOLD
61
SAWTOOTH WAVE FOR LSB PROCESSING
CLOCK EDGES OF THE MSB PROCESSING

FIG. 5

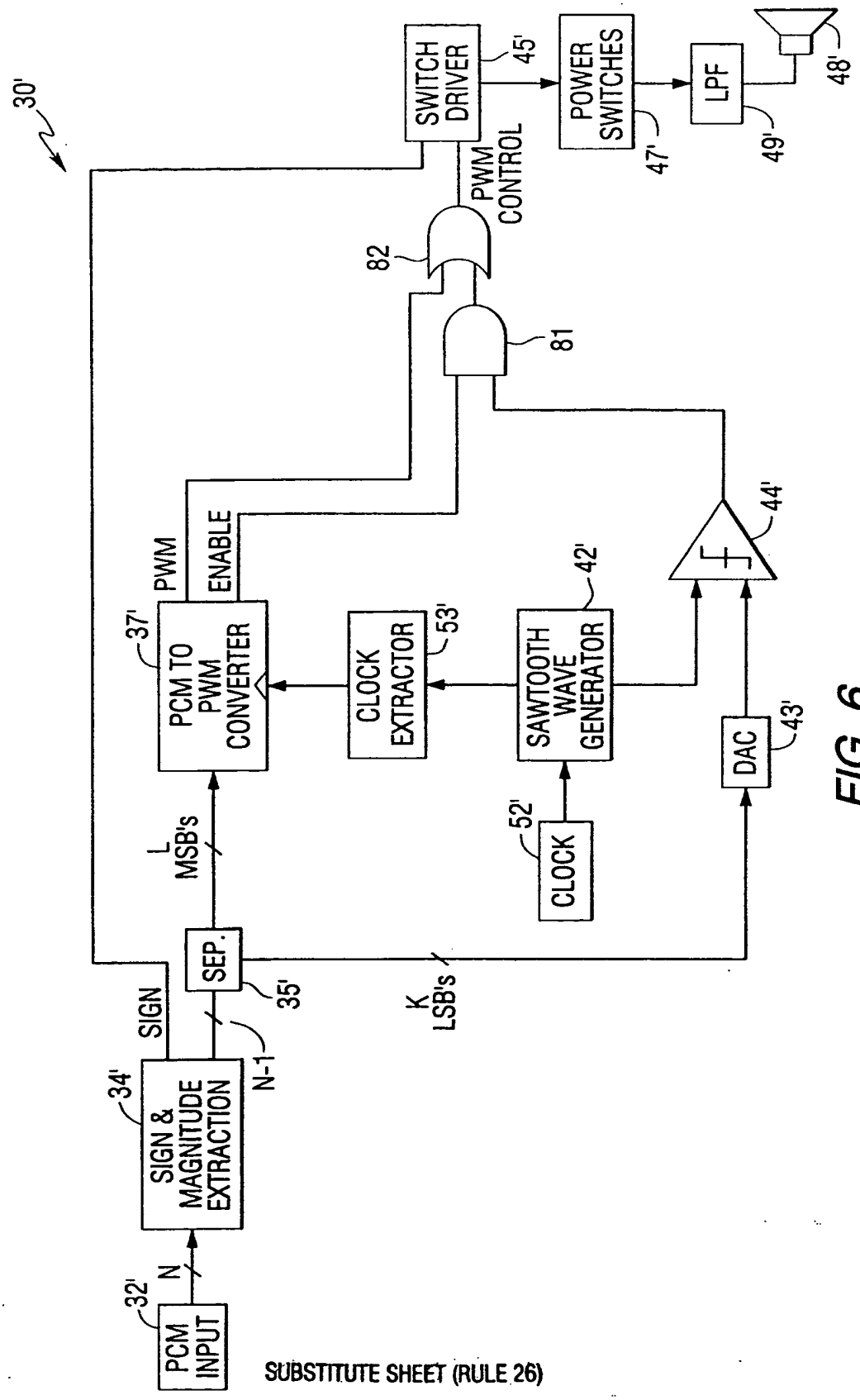
30'
SWITCH DRIVER
45'
POWER SWITCHES
47'
LPF
49'
48'
PWM CONTROL
82
81
44'
42'
PWM
ENABLE
37'
PCM TO PWM CONVERTER
CLOCK EXTRACTOR
53'
SAWTOOTH WAVE GENERATOR
DAC
43'
52'
CLOCK
L MSB's
SEP.
35'
K LSB's
SIGN
N-1
34'
SIGN & MAGNITUDE EXTRACTION
N
32'
PCM INPUT

FIG. 6

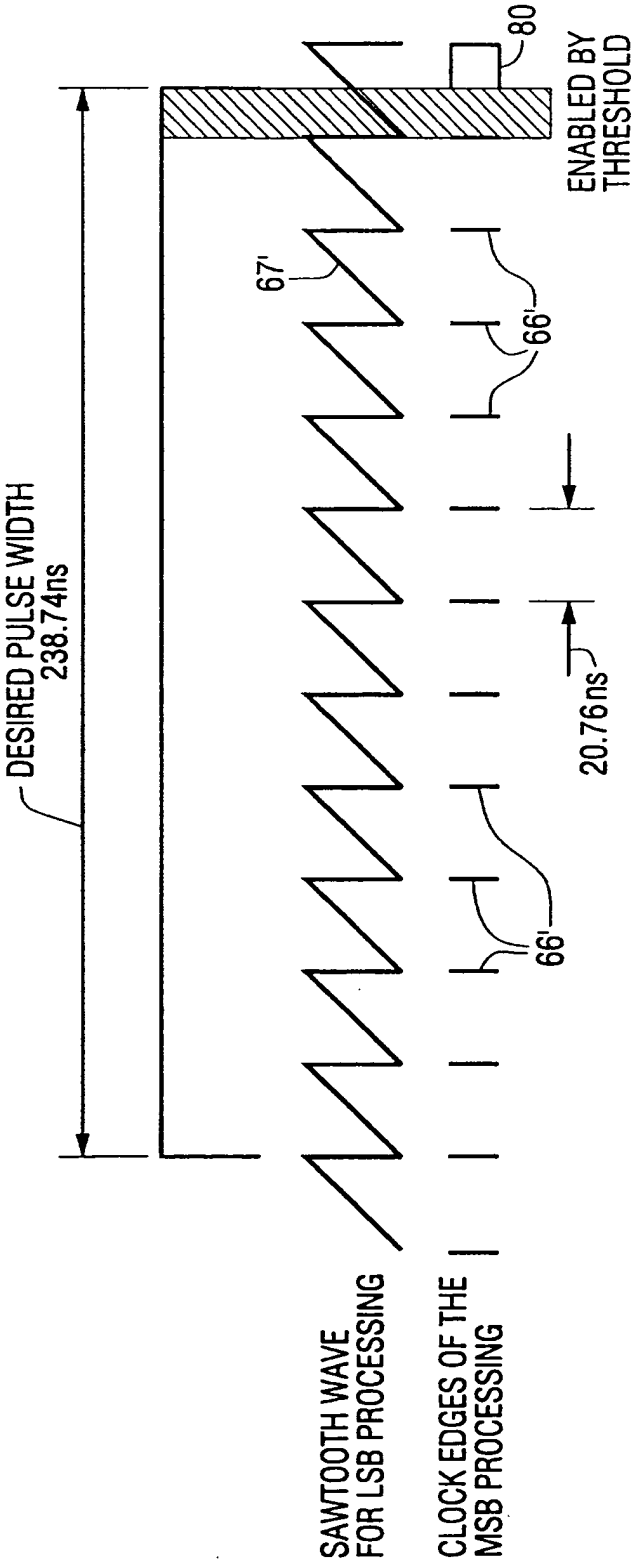
80
ENABLED BY THRESHOLD
67'
66'
66'
DESIRED PULSE WIDTH
238.74ns
20.76ns
SAWTOOTH WAVE FOR LSB PROCESSING
CLOCK EDGES OF THE MSB PROCESSING

FIG. 7

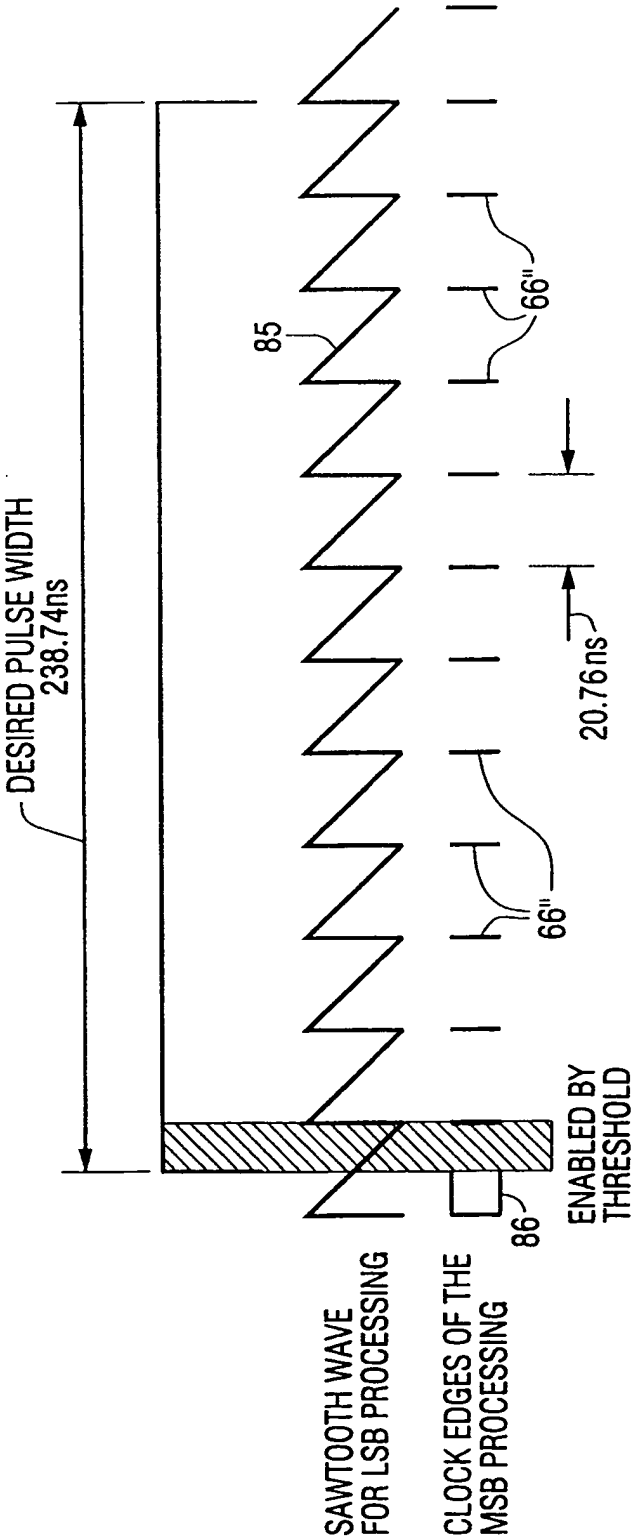
DESIRED PULSE WIDTH
238.74ns
85
66"
66"
20.76ns
ENABLED BY
THRESHOLD
86
SAWTOOTH WAVE
FOR LSB PROCESSING
CLOCK EDGES OF THE
MSB PROCESSING

FIG. 8

INTERNATIONAL SEARCH REPORT

Interna il Application No
PCT/US 99/07481

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H03M1/68 H03F3/217

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H03M H03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 4 590 457 A (AMIR GIDEON) 20 May 1986 see column 4, line 49 - column 6, line 10; figures 2A-2E	1
A	"PULSE WIDTH MODULATION SIGNAL GENERATOR" IBM TECHNICAL DISCLOSURE BULLETIN, vol. 37, no. 12, 1 December 1994, pages 499-501, XP000487868 see page 499, line 1 - page 50, line 4; figures 1-3	1
A	US 4 390 849 A (MISKIN LESLIE) 28 June 1983 see abstract; figures 1,2	1

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
5 July 1999	12/07/1999

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Beindorff, W

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

Intern: al Application No
PCT/US 99/07481

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 4590457 A	20-05-1986	JP 61016626 A	24-01-1986
US 4390849 A	28-06-1983	DE 3017414 A	12-11-1981
		EP 0039430 A	11-11-1981
		JP 57005408 A	12-01-1982